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EXAMINER	
SHAH, CHIRAG G	

ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/780,979	SMITH ET AL.	
	Examiner	Art Unit	
	Chirag G. Shah	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/9/01* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 6/29/05 have been fully considered but they are not persuasive.

Applicants argue that none of the applied references are understood to disclose or suggest at least the features of a communications device or controller implemented in an integrated circuit that includes memory for storing data and instructions. Applicants further contends that while Gotze describes the individual components as being inter-connected, nothing in Gotze is understood to teach or event suggest that these components are implemented in an integrated circuit. Examiner respectfully disagrees with the Applicant and redirects Applicant to the Gotze reference, specifically to fig. 4, and the respective section of col. 5, lines 27-38 of the specification. Gotze clearly discloses not only of individual components as being inter-connected, but integrated as one circuit into a device for controlling a data bus. The integrated (circuit) component 500 can control an R2-232 bus, CAN, ABUS and data bus 520 using respective drivers. The integrated component 500 works with data from the program and data memory. Gotze clearly describes component 500 as being an "integrated component," and the component 500 is a PowerPC micro-controller, which one skilled in the art would recognize as an integrated circuit having communication circuits, memory and processor as clearly disclosed in fig. 4. Therefore, claim 1 respectfully remains unpatentable over Jundt in view of Gotze.

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3-11, 14-19, 21-22, and 24-26 rejected under 35 U.S.C. 103(a) as being unpatentable over Jundt et al. (U.S. Patent No. 6,618,630), hereinafter referred as, Jundt in view of Gotze et al. (U.S. Patent No. 5,941,966), hereinafter referred as Gotze.

Referring to claims 1 and 16, Jundt discloses in figure 1 of a communication controller 12 comprising: a memory circuit [as disclosed in figure 1 and in column 4, lines 41 to 45];

a processor operable in response to data and instructions stored in the memory circuit [as disclosed in column 4, lines 41 to 45];

a first communication circuit [first of the plurality of I/O cards 22; the controller 12 communicates with the field devices 18 via any desired or standard I/O Cards 22, the I/O cards 22 may be analog I/O cards that connect the controller 12 to the field devices 18 may be digital or combined digital and analog and analog I/O cards that communicate using any desired format or protocols as disclosed in column 4, lines 41 to column 5, lines 18] under control of the processor 30 for communicating between the communication controller 12 and a first remote device 18 according to a first data communication standard [any desired format such as HART, PROFIBUS, WORLDFIP, DeviceNet and CAN; as disclosed in figure 1, claim 1, and column 4, lines 5 to column 5, lines 18]; and

a second communication circuit [second of the plurality of I/O cards 22] under control of the processor 30 for communicating between communication controller 12 and a second remote device [second one of the plurality of field device 18 as in figure 1]according to a second data communication standard [any desired format such as HART, PROFIBUS, WORLDFIP, DeviceNet and CAN; as disclosed in figure 1, claim 1, and column 4, lines 5 to column 5, lines 18], the second data communication standard being different from the first data communication standard [as disclosed in column 4, lines 5 to column 5, lines 18, any desired format may be used for communication between the controller 12 and device 18, thus first may use PROFIBUS and second may use CAN].

Jundt fails to disclose wherein the communication controller is integrated in a single integrated circuit.

Gotze discloses in the abstract of an apparatus using a plural level processor for controlling a data bus. Gotze discloses in figures 2 and col. 3, lines 21-44 of a device 200 for controlling a number of data buses 201, 202, 203, and 204. The controller device 200 is integrated in a single integrated circuit that includes memories (223,224), a plurality of processors (221, 222, which carry out separate and distinct control function from one another), which are connected to the data buses 201-204 via respective drivers. Furthermore, as disclosed in figure 2, the controlling device 200 further includes a micro-controller 230, which is connected to the processors 221 and 222 as shown. In addition, as disclosed in figure 4, col. 5, lines 27-38, the micro-controller 500 integrated into a device controls data buses, this integrated component 500 can control an R2-232, CAN, ABUS data buses using a corresponding drivers.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include into Jundt's invention the communication controller integrated in a single integrated circuit as taught by Gotze. One is motivated as such in order (as disclosed in col. 2, lines 42-62) to achieve high signal processing speed using simple circuit engineering, while partitioning of control tasks to different processor within an integrated circuit, permits an adaptation to new data bus types and their associated data bus protocol which is economical in both time and money.

Referring to claims 3, 4, 17 and 18, Jundt discloses wherein the first communication circuit comprises a ProfiBus or CAN circuit controller for external communication according to ProfiBus or CAN communication protocol [see figure 1 and column 4, lines 41 to 66, the controller 12 communicates with the field devices 18 via any desired or standard I/O cards 22,

the first of the plurality of I/O card 22 may communicate with field device using PROFIBUS or CAN] as claims.

Referring to claims 5, where in the second communication circuit comprises an Ethernet bus controller [as in figure 1 and column 3, lines 56 to column 4, lines 66] as claim.

Referring to claims 6 and 7, Jundt discloses wherein the second circuit comprises the CAN bus controller having a logic circuit configured to receive and transmit data according to the CAN standard [see figure 1, column 4, lines 5-66] as claim.

Referring to claim 9, Jundt disclose of an Ethernet bus controller under control of the processor for communicating between the communication controller and a third remote device according to Ethernet data communication standard [see figure 1 and column 3, lines 56 to column 4, lines 4 and column 4, lines 41-66] as claim.

Referring to claim 19, Jundt discloses in col. 4, lines 41-55 wherein the processing means [controller having a processor, see col. 4, lines 41-45] comprises: a processor coupled to the first communication means [first of the I/O cards 22] and the second communication means [second of the I/O cards 22].

Referring to claim 21, Jundt disclose:

a processor block which controls operation of the integrated circuit [figure 1 and column 3, lines 56 to column 4, lines 66];

a memory block which stores data and instructions for use by the processor block [as disclosed in figure 1 and in column 4, lines 41 to 45];

a first data communication port [first of the plurality of I/O cards 22; the controller 12 communicates with the field devices 18 via any desired or standard I/O Cards 22, the I/O cards 22 may be analog I/O cards that connect the controller 12 to the field devices 18 may be digital or combined digital and analog and analog I/O cards that communicate using any desired format or protocols as disclosed in column 4, lines 41 to column 5, lines 18];

a ProfiBus control block coupled with the first data communication port [any desired format such as HART, PROFIBUS, WORLDFIP, DeviceNet and CAN; as disclosed in figure 1, claim 1, and column 4, lines 5 to column 5, lines 18];

a second data communication port [second of the plurality of I/O cards 22]; a Controller Area Network (CAN) control clock coupled with the second data communication port [any desired format such as HART, PROFIBUS, WORLDFIP, DeviceNet and CAN; as disclosed in figure 1, claim 1, and column 4, lines 5 to column 5, lines 18]; and

Jundt discloses in column 4, lines 41-45 that the controller includes memory and processor that executes the process control solution and that controller communicates with the field device via CAN or any desired standard I/O device 22, but fails to explicitly discloses of an integrated circuit comprising an internal bus coupling the processor block, the memory block the Profibus control block and the CAN control block.

Gotze discloses in figure 2 and respective portion of the specification of a controller having a processor (221 or 222) that communicates via the internal bus with a memory (223 or 224) and with the Drivers 1-4. The controller device 200 is integrated in a single integrated circuit that includes memories (223,224), a plurality of processors (221, 222, which carry out separate and distinct control function from one another), which are connected to the data buses 201-204 via respective drivers. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include the teachings of communication within the controller via an internal bus as taught by Gotze. One is motivated as such in order to make communication within devices/circuits of the controller executable.

Referring to claim 24, Jundt discloses in figure 1 of a ProfiBus controller 12 comprising:

a ProfiBus core [first of the plurality of I/O cards 22; the controller 12 communicates with the field devices 18 via any desired or standard I/O Cards 22, the I/O cards 22 may be analog I/O cards that connect the controller 12 to the field devices 18 may be digital or combined digital and analog and analog I/O cards that communicate using any desired format or protocols as disclosed in column 4, lines 41 to column 5, lines 18];

a processor [as disclosed in column 4, lines 41 to 45];

a memory [as disclosed in figure 1 and in column 4, lines 41 to 45];;

at least one control circuit which controls wireline data communication according to a standard other than ProfiBus standard [the controller 12 communicates with the field devices 18 via any desired or standard I/O Cards 22, the I/O cards 22 may be analog I/O cards that connect the controller 12 to the field devices 18 may be digital or combined digital and analog and analog

I/O cards that communicate using any desired format or protocols as disclosed in column 4, lines 41 to column 5, lines 18 and further more control circuit controls wireline data communication to field device 18 in any desired format such as HART, PROFIBUS, WORLDFIP, DeviceNet and CAN as disclosed in figure 1, claim 1, and column 4, lines 5 to column 5, lines 18] as claim. Jundt discloses in figure 1 and respective portions of the specification that controller 12 may communicate using ProfiBus standard, but fails to explicitly disclose of an internal bus for internal data communications within the ProfiBus controller, where the ProfiBus controller is integrated in an integrated circuit.

Gotze discloses in figures 2 and col. 3, lines 21-44 of a device 200 for controlling a number of data buses 201, 202, 203, and 204. Gotze discloses in figure 4 of an integrated component 500 within a control device of figure 2, may control a further data bus (which may be Profibus according to col. 2, 1-8) via driver 521. Gotze further discloses in figure 2 of an internal bus communication within the device 200, where as mentioned before, the ProfiBus controller being another data bus is integrated in an integrated circuit.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include into Jundt's invention the communication controller integrated in a single integrated circuit as taught by Gotze. One is motivated as such in order (as disclosed in col. 2, lines 42-62) to achieve high signal processing speed using simple circuit engineering, while partitioning of control tasks to different processor within an integrated circuit, permits an adaptation to new data bus types and their associated data bus protocol which is economical in both time and money.

Referring to claims 8, 22 and 26, Gotze discloses in figure 4 of a first CAN control block 510 and other control block 520, which can serve as second CAN control block. Gotze discloses in figure 2 of drivers associated with the respective Bus of Figure 4 are coupled to the internal bus.

Referring to claims 10, 11, and 15, Gotze discloses wherein the CAN bus controller comprises two or more asynchronous serial data communication circuits [Figure 4, RS-232 515 and other 520 server as two or more asynchronous serial data communication circuits].

Referring to claim 14, Gotze discloses in figure 4 of further comprising wherein the memory circuit comprises a boot read only memory (550s) and read-write memory (VRAM).

Referring to claims 25, Jundt discloses wherein the second circuit comprises the CAN bus controller having a logic circuit configured to receive and transmit data according to the CAN standard [see figure 1, column 4, lines 5-66] as claim.

5. Claims 12, 13, 20, 23, and 27-29 rejected under 35 U.S.C. 103(a) as being unpatentable over Jundt in view of Gotze as applied to claims 1, 3-11, 14-19, 21-22, and 24-26 above, and further in view of NetSilicon (NET+12).

Referring to claim 12, Jundt discloses in figure 1 and in column 3, lines 56 to column 4, lines 66 of the processor, the first communication circuit, the second communication circuit and

the Ethernet bus controller. Jundt in view of Gotze fails to explicitly disclose of an internal communication bus coupled to the processor, the first communication circuit, the second communication circuit and the Ethernet bus controller. NetSilicon discloses in the NET+12 Processor Block Diagram and in the Hardware Specification portion of the specification of a controller having a fully integrated processor that communicates via the internal bus with a memory and Integral 10/100 Ethernet interface and with the I/O ports. The memory holds a control program for the controlled process, an operating system, and programming for execution. Therefore, it would have been obvious to one of ordinary skill in the art to include the teachings of communication within the controller via an internal bus as taught by NetSilicon into Jundt in view of Gotze's invention in order to make communication within devices/circuits of the controller executable.

Referring to claim 13, Jundt in view of Gotze fails to disclose a communication controller comprising a SPI bus controller. NetSilicon discloses of an Embedded Ethernet/Internet-Ready Processor and discloses on the NET+12 Processor Block Diagram and in the Hardware Specification section of further comprising a DMA controller having 4 dedicated channels for a Serial Peripheral Interconnect (serial transmit and receive) bus controller as claim. Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to modify the teachings of Jundt in view of Gotze to include an controller comprising an SPI bus controller as taught by NetSilicon in order to support multitude of different transmission protocols in a fully integrated solution.

Referring to claim 20, NetSilicon discloses in the NET+12 Processor Block Diagram and in the Hardware Specification of further comprising: an interface means for serial communication (2 Serial Port) with an external data source for loading at least a portion of the memory (Programmable Memory Controller) means upon initialization of the data communication device.

Referring to claims 23 and 27, NetSilicon discloses in the NET+12 Processor Block Diagram of an Integral 10/100 Ethernet MAC control block coupled to the internal bus.

Referring to claim 28, NetSilicon discloses in the NET+12 Processor Block Diagram wherein the processor comprises a serial communication port (2 Serial Ports, Asynchronous and Synchronous Serial Data and Control) for external data communication as claim.

Referring to claim 29, NetSilicon discloses in the NET+12 Processor Block Diagram and in the Hardware Specification of further comprising: program code stored in a first portion of the memory (SRAM) and executable by the processor (RSIC Processor) for controlling loading of data and instructions from an external data source by the serial communication port (2 Serial Port) to a second portion of memory (ROM).

6. Claims 30-34 rejected under 35 U.S.C. 103(a) as being unpatentable over Jundt in view of Net Silicon (NET+12).

Referring to claim 30-31, Jundt discloses in figure 1 and column 3, lines 56 to column 4, lines 66 of a communication controller 12, fabricated on a circuit, for communication between at least two devices (one of workstations 14 and field device 18), comprising: a plurality of interface circuits comprising:

an Ethernet Interface circuit for communication using Ethernet communication standard [see figure 1 and column 3, lines 56 to column 4, lines 4];

a Controller Area Network interface circuit for communication using a Controller Area Network communication standard [see figure 1 and column 4, lines 41 to 66];

a processor [as disclosed in column 4, lines 41-45] for controlling the communication between the communication controller 12 and a first device 14 using a first interface circuit [Ethernet as disclosed in column 3, lines 56 to column 4, lines 4] of the plurality of interface circuits and between the communication controller 12 and a second device 18 [I/O cards 22 using any desired protocol or format such as HART, PROFIBUS, WORLDFIP, DeviceNet and CAN as disclosed in column 4, lines 41 to 66 using a second interface circuit of the plurality of interface circuits, wherein the first circuit [Ethernet] is different from the second interface circuit [any desired protocol or format such as HART, PROFIBUS, WORLDFIP, DeviceNet and CAN] as claim.

Jundt discloses of a controller 12 having memory for storing operating instructions for execution by processor in column 4, lines 41-45 but fails to explicitly disclose of the memory comprising volatile and non-volatile memory. Jundt further fails to disclose of having a communication controller fabricated as an integrated circuit and having an option to select a

Serial Peripheral Interface Circuit for communication using a SPI communication standard among the other desired formats or protocols.

NetSilicon discloses of an Embedded Ethernet/Internet-Ready Processor and discloses in paragraph 1 of the first page, the NetSilicon NET+12 is a high-performance highly integrated 32-bit microprocessor having DMA controller, Ethernet MAC controller and memory controller among a plurality of communication standards designed for use in networked devices. NetSilicon further discloses on the NET+12 Processor Block Diagram and in the Hardware Specification section of further comprising a DMA controller having 4 dedicated channels for a Serial Peripheral Interconnect (serial transmit and receive) bus controller. NetSilicon additionally discloses in the NET+12 Processor Block Diagram of the controller having a Programmable Memory Controller block supporting ROM and SRAM having the functionality of volatile and non-volatile memory.

Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to modify the teachings of Jundt to include the features of SPI, ROM and SRAM in the controller fabricated as an integrated circuit as taught by NetSilicion. One is motivated as such in order to ensure complete scalability and compatibility for supporting a plurality of communication standard in use today, while assuring a reliable network performance.

Referring to claims 32-33, Jundt discloses in figure 1 and column 3, lines 56 to column 4, lines 66 a communication controller 12, fabricated on a circuit, for communication between at least two devices (one of workstations 14 and field device 18), comprising:

a plurality of interface circuits selected from a group consisting of an Ethernet Interface circuit for communication using Ethernet communication standard; a Controller Area Network interface circuit for communication using a Controller Area Network communication standard; and a field bus interface circuit for communication using a fieldbus communication standard, wherein at least two of the interface circuits are different [the controller 12 communicates with the field devices 18 via any desired or standard I/O Cards 22, the I/O cards 22 may be analog I/O cards that connect the controller 12 to the field devices 18 may be digital or combined digital and analog and analog I/O cards that communicate using any desired format or protocols as disclosed in column 4, lines 41 to column 5, lines 18, format such as HART, PROFIBUS, WORLDFIP, DeviceNet and CAN; as disclosed in figure 1, claim 1, and column 4, lines 5 to column 5, lines 18];

a processor [as disclosed in column 4, lines 41-5] for controlling the communication between the communication controller 12 and a first device 14 using a first interface circuit [Ethernet] the plurality of interface circuits and between the communication controller 12 and a second device 18 using a second interface circuit of the plurality of interface circuits, wherein the first circuit is different from the second interface circuit [I/O cards 22 using any desired protocol or format such as HART, PROFIBUS, WORLDFIP, DeviceNet and CAN as disclosed in column 4, lines 41 to 66 using a second interface circuit of the plurality of interface circuits, wherein the first circuit [Ethernet] is different from the second interface circuit [any desired protocol or format such as HART, PROFIBUS, WORLDFIP, DeviceNet and CAN] as claim] and

a processor for controlling the communication between the communication controller 12 and a first device 14 using the Ethernet interface circuit [as disclosed in column 3, lines 56 to

column 4, lines 4] and between the communication controller 12 and a second device 18 using the fieldbus interface circuit [as disclosed in column 4, lines 41-66].

Jundt discloses of a controller 12 having memory for storing operating instructions for execution by processor in column 4, lines 41-45 but fails to explicitly disclose of the memory comprising volatile and non-volatile memory. Jundt further fails to disclose of having a communication controller fabricated as an integrated circuit and having an option to select a Serial Peripheral Interface Circuit for communication using a SPI communication standard among the other desired formats or protocols.

NetSilicon discloses of an Embedded Ethernet/Internet-Ready Processor and discloses in paragraph 1 of the first page, the NetSilicon NET+12 is a high-performance highly integrated 32-bit microprocessor having DMA controller, Ethernet MAC controller and memory controller among a plurality of communication standards designed for use in networked devices. NetSilicon further discloses on the NET+12 Processor Block Diagram and in the Hardware Specification section of further comprising a DMA controller having 4 dedicated channels for a Serial Peripheral Interconnect (serial transmit and receive) bus controller. NetSilicon additionally discloses in the NET+12 Processor Block Diagram of the controller having a Programmable Memory Controller block supporting ROM and SRAM having the functionality of volatile and non-volatile memory.

Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to modify the teachings of Jundt to include the features of SPI, ROM and SRAM in the controller fabricated as an integrated circuit as taught by NetSilicion. One is motivated as

such in order to ensure complete scalability and compatibility for supporting a plurality of communication standard in use today, while assuring a reliable network performance.

Referring to claim 34, Jundt discloses in figure 1 of communication controller 12 for communication between at least two devices (14 and 18), comprising:

a processor [as disclosed in column 4, lines 41-45], and

a memory [as disclosed in column 4, lines 41-45] for storing operating instructions for execution by the processor to control communication using a plurality of communication standards selected from the group consisting of an Ethernet communication standard [as disclosed in column 3, lines 56 to column 4, lines 4], a controller area network communication standard, and a fieldbus communication standard [as disclosed in column 4, lines 5 to 66] ,

wherein the processor controls communication between the communication controller 12 and a first device 14 using a first communication standard [Ethernet as disclosed in column 3, lines 56 to column 4, lines 4] of the plurality of communication standards and between the communication controller 12 and a second device 18 using a second communication standard of the plurality of communication standards, where the first communication standard is different from the second communication standard [I/O cards 22 using any desired protocol or format such as HART, PROFIBUS, WORLDFIP, DeviceNet and CAN as disclosed in column 4, lines 41 to 66 using a second interface circuit of the plurality of interface circuits, wherein the first circuit [Ethernet] is different from the second interface circuit [any desired protocol or format such as HART, PROFIBUS, WORLDFIP, DeviceNet and CAN] as claim].

Jundt fails to disclose wherein the communication controller is fabricated as an integrated circuit and having an option to select a Serial Peripheral Interface Circuit for communication using a SPI communication standard among the other desired formats or protocols.

NetSilicon discloses of an Embedded Ethernet/Internet-Ready Processor and discloses in paragraph 1 of the first page, the NetSilicon NET+12 is a high-performance highly integrated 32-bit microprocessor having DMA controller, Ethernet MAC controller and memory controller among a plurality of communication standards designed for use in networked devices. NetSilicon further discloses on the NET+12 Processor Block Diagram and in the Hardware Specification section of further comprising a DMA controller having 4 dedicated channels for a Serial Peripheral Interconnect (serial transmit and receive) bus controller. NetSilicon additionally discloses in the NET+12 Processor Block Diagram of the controller having a Programmable Memory Controller block supporting ROM and SRAM having the functionality of volatile and non-volatile memory.

Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to modify the teachings of Jundt to include the features of SPI, ROM and SRAM in the controller fabricated as an integrated circuit as taught by NetSilicion. One is motivated as such in order to ensure complete scalability and compatibility for supporting a plurality of communication standard in use today, while assuring a reliable network performance.

Conclusion

Any response to this final action should be faxed to:

(571-272-8300), (for formal communications; please mark "EXPEDITED PROCEDURE)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chirag G. Shah whose telephone number is 571-272-3144. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 571-272-3134. The fax phone number for the organization where this application or proceeding is assigned is 571-272-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

cgs
September 6, 2005

Ajit Patel
Primary Examiner